Notice of Allowability	Application No.	Applicant(s)	
	09/211,718	FOSSUM ET AL.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/20/2005*.

2. ☒ The allowed claim(s) is/are *1-13,17-22(The claims have been renumbered as 1-19 respectively)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Peter Mcgee on August 22, 2005.

2. The application has been amended as follows:

a. Claim 8: lines 2-8, change "providing at least two image sensor chips, each chip having first and second parallel edges and an image sensor array of imaging pixels that comes within two pixel pitches of said first and second edges, and includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array between said first and second edges; abutting said image sensor chips along at least one of corresponding first and second edges; and." to "providing at least two image sensor chips, each chip having first and second parallel edges, **a third edge aligned transverse to said first and second edges,** and an image sensor array of imaging pixels that comes within two pixel pitches of said **first, second, and third edges**, and includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array between said first and second edges; abutting said image sensor chips along at least **a respective** one of **said** first and second edges; and"

b. Claim 9: line 6, change "parallel edges including a third edge and a fourth edge; and" to "parallel edges including a third edge **aligned transverse to said first and second edges; and**

c. Claim 9: lines 9-12, change "forming said CMOS image sensor portion and thereby forming at least two sensor areas, said control portion including a pixel interpolator located between said at least two image sensor areas and one of said edges of said first CMOS image sensor chip." to "forming said CMOS image sensor portion and thereby forming at least two sensor areas **including a first sensor area extending to within a few pixel pitches of said first and third edges, and a second area extending to within a few pixel pitches of said second and third edges**, said control portion including a pixel interpolator located between said at least two image sensor areas and one of said edges of said first CMOS image sensor chip".

Drawings

3. The drawings were received on 10/22/2003. These drawings are acceptable.

Allowable Subject Matter

4. Claims 1-13 and 17-22 are allowed.

5. The following is an examiner's statement of reasons for allowance: The prior art of record, neither anticipates nor renders obvious the following limitations as claimed:

[Claim 1]: A CMOS image sensor circuit, comprising "....said image sensor portion including imaging pixels extending between said first edge, said second edge, and said third edge, such that imaging pixels of said first area of said image sensor portion are adjacent said first edge and said

third edge of said chip and imaging pixels of said second area of said image sensor portion are adjacent said second edge and said third edge of said chip; said row logic being physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion; and a pixel interpolator and said chip driver circuitry located between said first area and said second area of said image sensor portion and said fourth edge of said chip." in combination with other claimed elements.

[Claim 9]: A CMOS imager comprising "...."forming said CMOS image sensor portion and thereby forming at least two sensor areas including a first sensor area extending to within a few pixel pitches of said first and third edges, and a second area extending to within a few pixel pitches of said second and third edges, said control portion including a pixel interpolator located between said at least two image sensor areas and one of said edges of said first CMOS image sensor chip" in combination with other claimed elements.

[Claim 8]: A method of capturing an image, comprising: providing at least two image sensor chips, each chip having first and second parallel edges, a third edge aligned transverse to said first and second edges, and an image sensor array of imaging pixels that comes within two pixel pitches of said first and second edges, and includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array between said first and second edges; abutting said image sensor chips along at least a respective one of said first and second edges; and interpolating missing pixels on said chips, the missing pixels being caused by both said row select logic and by spaces between pixel pitches along abutted edges of said image sensor chips.

Claims 11, 13 and 17 are allowable and are deemed to avoid the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
September 9, 2005

DAVID L. OMETZ
SUPERVISORY PATENT
EXAMINER